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# Implementation of Solar Tracking in Robotic System Using Gate Array

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***Abstract:*** **This paper proposes an FPGA-based implementation of an MPPT control system suitable for stereovision robot. At the core of this system, the Perturb-and-observe algorithm is used to track the maximum power point. The algorithm runs on an Altera FLEX 10K FPGA chip. Additional functional blocks, such as the ADC interface, FIR filter, dither generator, and DAC interface, needed to support the MPPT control system are integrated within the same FPGA device thus streamlining the part composition of the physical prototype used to build this control system.**

***Keywords:*** **field-programmable gate arrays (FPGA), maximum power point tracking (MPPT), digital signal processors (DSPs), photovoltaic (PV) arrays, Stereovision Robot.**

## I. INTRODUCTION

Satellites need a source of power throughout their missions to help them remain operational for several years. The power supplies of these satellites, provided primarily by solar arrays, must have high efficiencies and low weights in order to meet stringent design constraints. Power conversion from these arrays is required to provide robust and reliable conversion which performs optimally in varying conditions of peak power, solar flux, and occlusion conditions. Since the role of these arrays is to deliver power, one of the principle factors in achieving maximum power output from an array is tracking and holding its maximum-power point. This point, which varies with temperature, insolation, and loading conditions, must be continuously monitored in order to react to rapid changes.

Until recently, the control of maximum power point tracking (MPPT) has been implemented in microcontrollers and digital signal processors (DSPs). While DSPs can provide a reasonable performance, they do not provide the advantages that field-programmable gate arrays (FPGA) chips can potentially offer to the implementation of MPPT control. In comparison to DSP implementations, FPGAs offer lower cost implementations since the functions of various components can be integrated onto the same FPGA chip as opposed to DSPs which can perform only DSP-related computations. In addition, FPGAs can provide equivalent or higher performance with the customization potential of an ASIC. Because FPGAs can be reprogrammed at any time, repairs can be performed in-situ while the system is running thus providing a high degree of robustness.

Beside robustness, this reprogrammability can provide a high level of (i) flexibility that can make upgrading an MPPT control system easy by merely updating or modifying the MPPT algorithm running on the FPGA chip, and (ii) expandability that makes expanding an FPGA-based MPPT control system to handle multi-channel control. In addition, this reprogrammability provides a level of testability that DSPs cannot match by allowing the emulation of the entire MPPT control system onto the FPGA chip.

Maximum power point tracking (MPPT) is a technique that grid-tie inverters, solar battery chargers and similar devices use to get the maximum possible power from one or more photovoltaic devices, typically solar panels. Since the role of PV arrays is to deliver power, one of the principle factors in achieving maximum power output from an array is tracking and holding its maximum-power point. This point, which varies with temperature, insolation, and loading conditions, must be continuously monitored in order to react to rapid changes. Until recently, the control of maximum power point tracking (MPPT) has been implemented in microcontrollers and digital signal processors (DSPs). While DSPs can provide a reasonable performance, they do not provide the high degree of flexibility that field-programmable gate arrays (FPGA) chips offer today. In comparison to DSP implementations, FPGAs offer equivalent or higher performance with the

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customization potential of an ASIC. From an implementation perspective, FPGAs provide designers with a significantly finer grain of control at the design level, which can lead to highly optimized implementations. As a case in point, it is possible to do more with less by running the system at a slower clock frequency to conserve power. As FPGA chips migrate to nanometer-range CMOS processes, they gain considerably in gate capacity, clocking speed and programming flexibility

## II. FPGA TECHNOLOGY

Field-Programmable Gate Arrays (FPGAs) are a member of the Programmable Logic Device (PLD) family. They are characterized by an array of logic cells surrounded by a highly configurable interconnect structure. Depending on the particular FPGA family, the size and complexity of the logic cells will vary, as will the number and type of interconnects throughout the device. Some devices also include RAM blocks which can be configured as part of a design. The remainder of this section will focus on Altera devices since the FPGA implementation described in this thesis is based on an Altera FPGA chip.

The Altera FLEX 10K series, used in this project, is comprised of a "sea-of-gates" architecture featuring a combination of Logic Array Blocks (LABs) and Embedded Array Blocks (EABs). These blocks are surrounded by row and column interconnects, which can be used to transport signals through the device. Each row of LABs contains a single EAB. The LABs and EABs are connected using a specialized FastTrack Interconnect designed for direct, high-speed communication

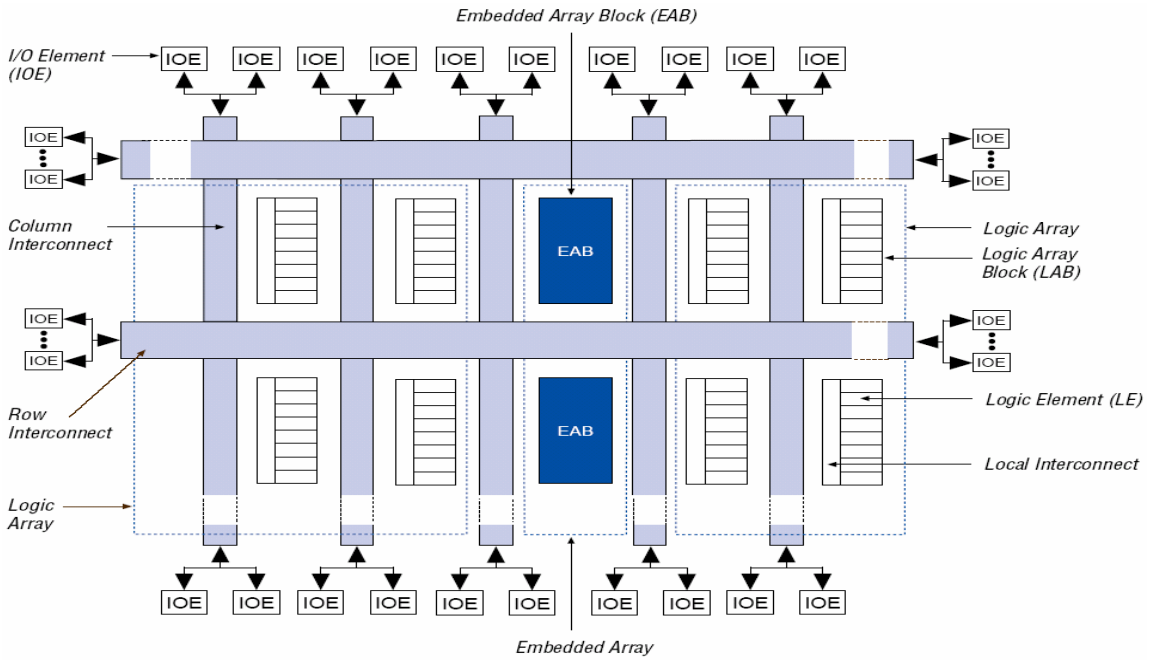


**Fig 1. Altera FLEX 10K device block diagram**

### A. Advantages of using FPGA Technology

(i) Until recently, all digital MPPT implementations have been based on DSP or microcontroller platforms. To our knowledge, this is the first FPGA implementation for MPPT control based on our search of the literature. This implementation presents a new development path which could yield lower costs and higher performance.

(ii) In general, a conventional microprocessor is capable of performing only a single instruction at any given time. In FPGA implementations, however, multiple copies of the MPPT algorithm can be running simultaneously, allowing multiple channels to be easily handled with a single device. This greatly simplifies communication and drastically reduces part counts.

(iii) In the pursuit of reduced costs and increased economic efficiency, some A/D and D/A concepts will be considered to see if they represent a feasible means of further utilizing the processing power of the FPGA to eliminate the external ADCs and DACs.

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(iv) By using the available computational resources and flexible programmability available in FPGA chips, a series of digital filters will be tested on the inputs in order to improve the effectiveness of the MPPT algorithm.

### B. MPPT System functionality

MPPT can be performed by using any algorithm which can adequately detect and follow the maximum power output of the solar array. Therefore, numerous algorithms have been proposed to support MPPT. This thesis considers the case of two algorithms, namely the Incremental Conductance (IncCond) algorithm and the Perturb-and-Observe (P&O) algorithm.

#### *1) The Incremental Conductance Algorithm*

The IncCond algorithm tracks the maximum power point by comparing the incremental and instantaneous conductances of the PV array. By sampling changes in the array voltage and current, the incremental conductance can be varied This essentially correlates to finding the point **where** ***dP/dV*=0** without applying a dither to the system. The IncCond algorithm is advantageous because it has no oscillation about the power point, thereby increasing efficiency. In general, it tracks the maximum power point effectively under rapidly changing conditions. However, this algorithm is usually disregarded as requiring too much computation for the amount of time allotted, thereby reducing the sampling frequency of the system

#### *2) The Perturb and Observe Algorithm*

Although it is regarded as less efficient than the IncCond algorithm in some studies, the P&O algorithm is the most commonly used algorithm for MPPT Essentially, a traditional hill-climbing approach is used to track the peak power output. Based on this point, it is known that on the left hand side of the curve, $\Delta P/\Delta V>0$. However, on the right hand side of the curve, $\Delta P/\Delta V<0$. Therefore, this differential will only be equal to zero at the peak of the power curve. Whenever the controller drifts away from the maximum, the reference voltage can be adjusted by a constant factor in the opposite direction. This only requires the values for voltage, current, and power from the previous iteration in order to calculate the differentials.

## III. SYSTEM ARCHITECTURE

The architecture of the MPPT system consists of a pipelined structure that facilitates efficient data flow from a starting point, represented by the ADCs, to a terminal point represented by the DACs. Allows its architectural blocks to be processing in parallel, yielding much higher utilization. The P&O algorithm runs on an Altera FPGA which embedded on an Altera UP2 development board. This board contains a Flex 10K70 FPGA with approximately 70,000 equivalent gates. The original oscillator of this board was replaced with another oscillator operating at 10 MHz. A daughterboard containing the necessary ADCs, which are single-input ADS8322 and DACs was designed to interface with this development board and the main DC-DC converter. The DACs are Texas Instruments DAC8544 with 4 separate outputs, capable of converting 16-bits within a maximum settling time of 10μs.

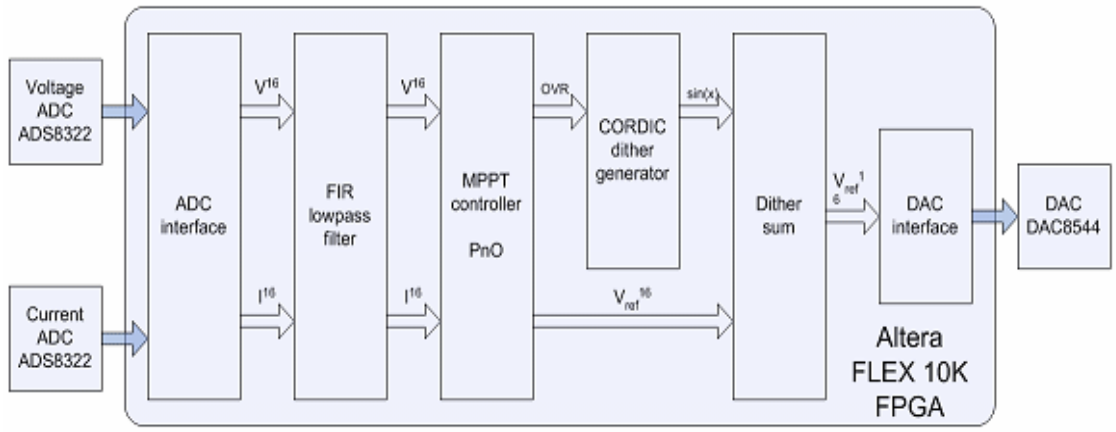


**Fig 2. Pipelined system architecture**

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The ADCs selected for this architecture are 16-bit Successive Approximation Register (SAR) devices from Texas Instruments designed to operate at a maximum of 500,000 samples per second. Beside the capability of handling parallel data, these components were selected to strike a balance of cost, speed, and ease of implementation.

## IV. SIMULATION RESULTS

To verify the system architecture, simulations were performed using Altera's Quartus II Web Edition, version 4.1 SP2. Each block was simulated for proper functionality before being tested in-circuit. Figure 25 shows the timing waveforms for the ADC controller, which controls both the current ADC and voltage ADC. Since the ADCs are Successive Approximation Register (SAR), a block is required for each bit sampled plus overhead. Therefore, 20 clock cycles are required to receive a value from the ADC. The clock is represented by clk, adc1_clk, and adc2_clk, while the signals adcX_busy, adcX_byte, adcX_convst, adcX_cs, and adcX_rd represent the busy flag, 8/16-bit data width flag, the conversion start flag, the chip select flag, and the read flag. Each ADC receives the same control signals. The sampled data is shown as dacX_data.

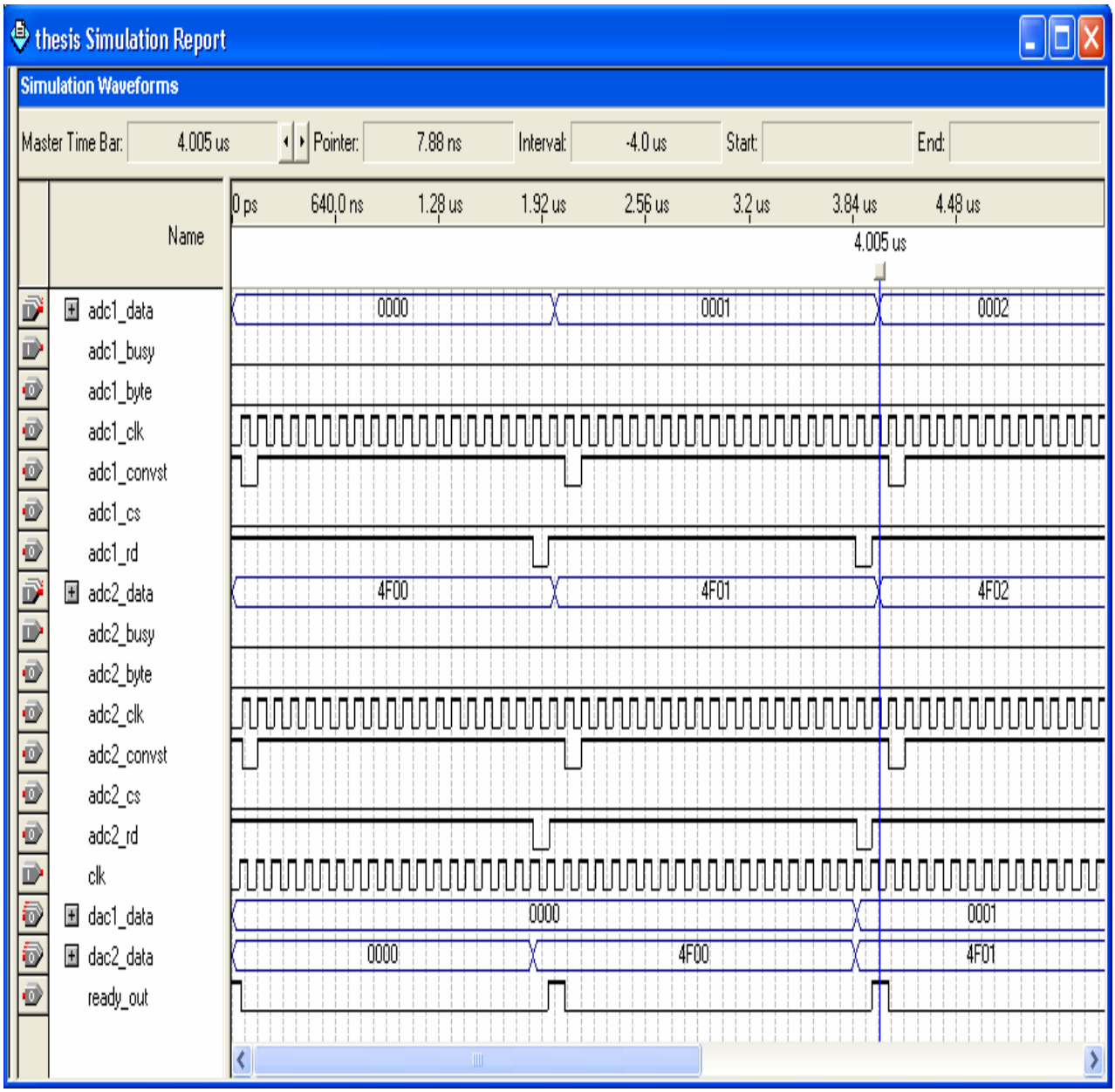


**Fig 3. Simulation results of ADC interface**

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Figure illustrates the simulation of the MPPT controller, the unit responsible for making the decisions regarding tracking. For each clock cycle that ready_in is high, the voltage and current are read, and the differentials are processed in order to make decisions about whether or not to track, and in what direction. The signals didv_test, dp_test, dv_test, mppt_dir, skip_mppt, and ovr are internal flags based upon each calculation and provide information about the decisions made by the algorithm. The modified Vref is sent out on vref_out

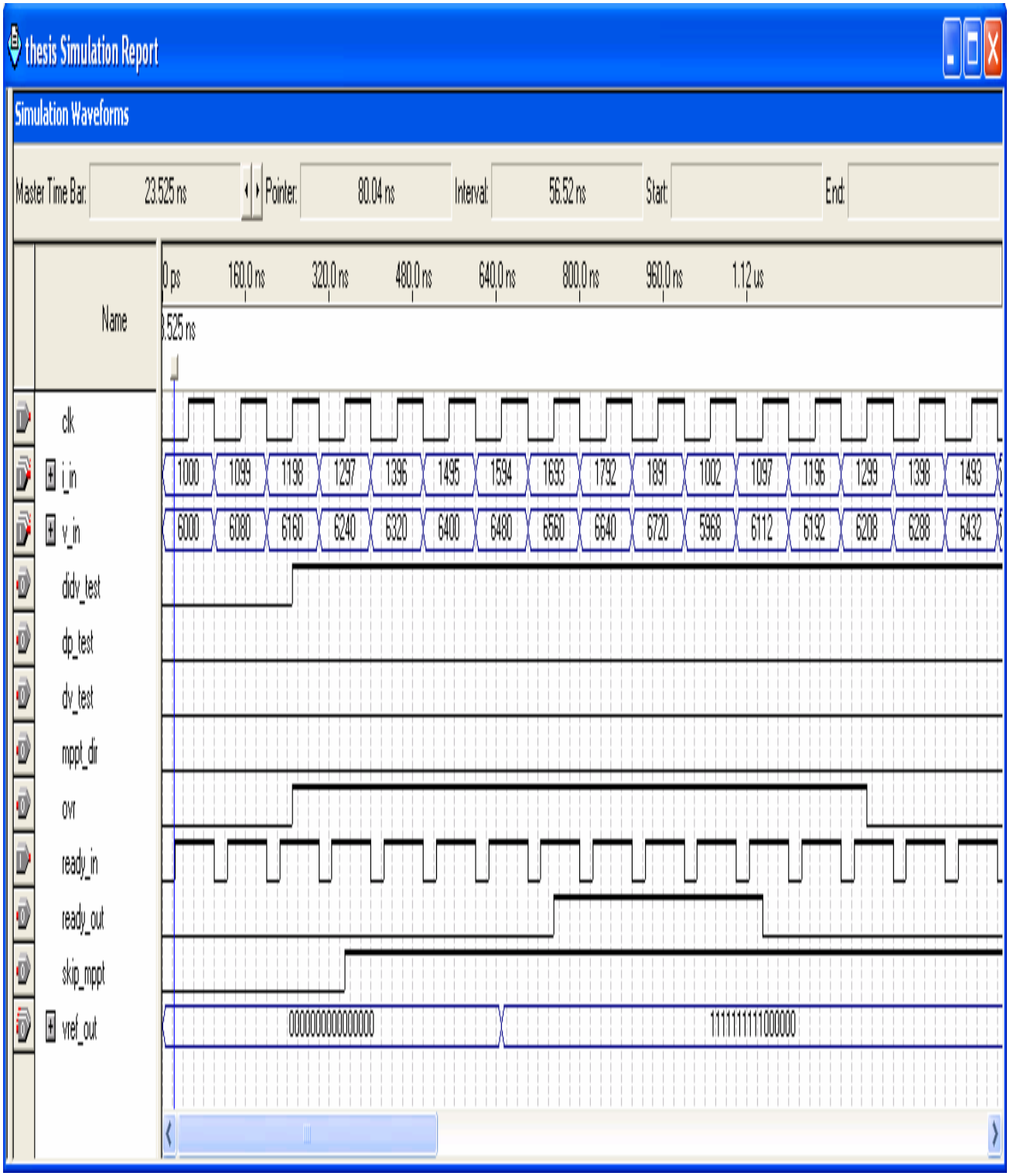


**Fig 4. Simulation results of MPPT controller.**

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The simulation data for the quad-output DAC controller. The internal voltage references and ramp generator are labelled as vgen1-4 and rampgen, respectively. The inputs to the block are dac_data_1 through dac_data_4. These inputs are sent to the DAC on dac_data in a sequential fashion, and the targeted DAC output is selected using address lines dac_a0 and dac_a1. Three clock cycles are required for a single output, therefore all four updates require 12 clock cycles. The remaining control signals dac_cs, dac_ldac, dac_pd, dac_rst, dac_rw represent the chip select, load DAC command, power-down, device reset, and read/write select flags, respectively.

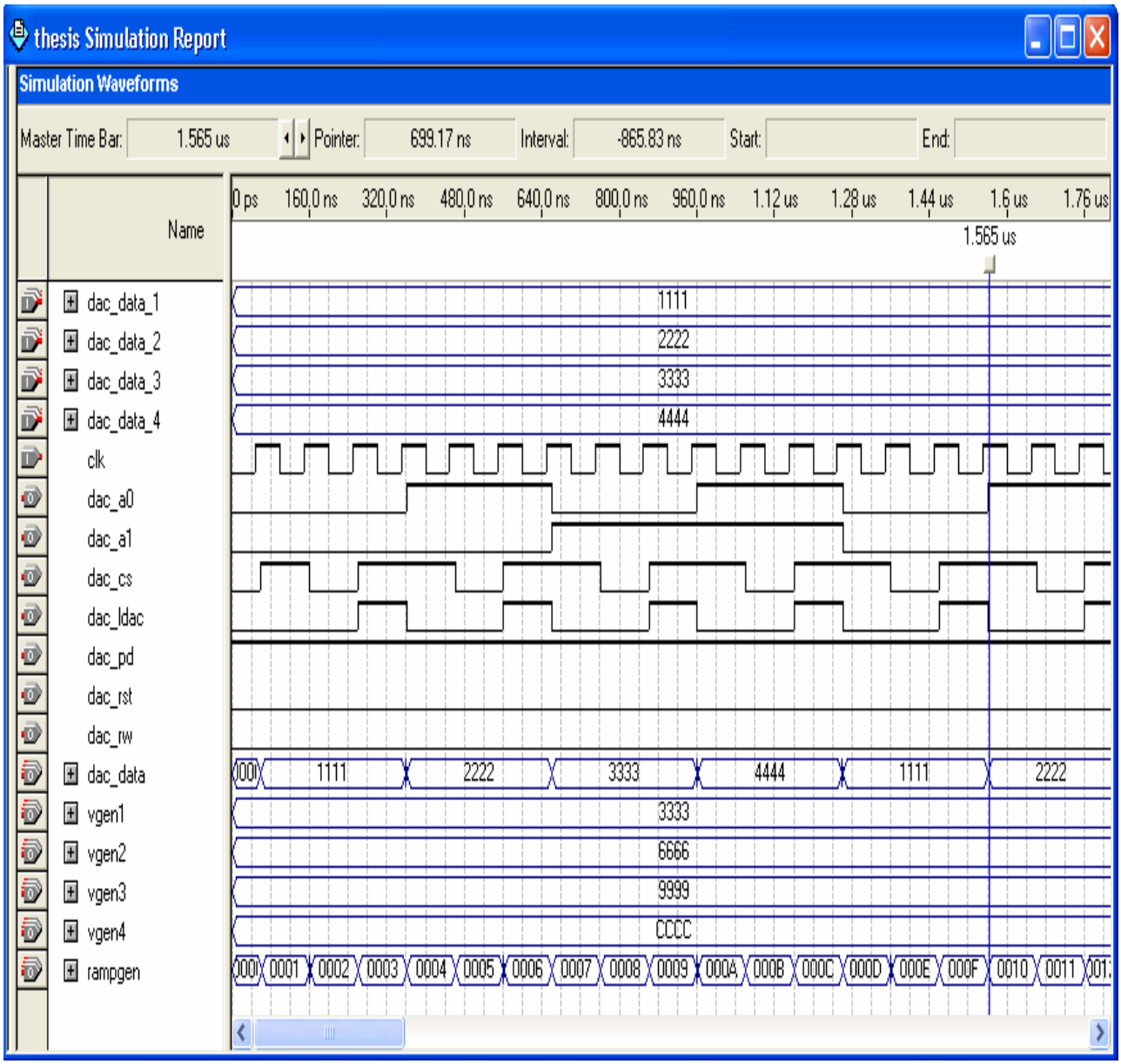


**Fig 5. Simulation results of DAC interface.**

## V. SYSTEM ARHITECTURE SYNTHESIS

After VHDL modelling, Altera's Quartus II Web Edition, version 4.1 SP2, was used to synthesize the different blocks in the system architecture. Table 3 shows the number of VHDL lines of code written to specify the functionality of each block, the number of LEs needed to implement each block in the FLEX chip, and the ratio of the implementation LEs to

the available LEs in the actual device. The device utilization is also given as a reference. The utilization figures are based on the Altera FLEX 10K70 device, which contains 3,744 LEs.

**Table 1: VHDL specification and synthesis of each block in the system architecture.**

| Module Name | Lines of VHDL | Logic Elements | Device Utilization(%) |
|---|---|---|---|
| ADC Controller | 123 | 52 | 1.39 |
| Downsampler | 76 | 141 | 3.77 |
| MPPT Controller | 403 | 825 | 22.04 |
| CORDIC | 140 + 37 | 681 | 18.19 |
| Dither Sum | 82 | 70 | 1.87 |
| DAC Controller | 163 | 100 | 2.67 |
| TOTAL | 1,024 | 1,869 | 49.92 |

As shown in this table, only half of the logic capacity of the FLEX 10K is used. Although this device is a low capacity chip, it is largely sufficient to implement an entire MPPT controller. This result makes the case for using high capacity chips for implementing complex controllers such as the ones used for multi-channel based on intelligent computational approaches such as neural networks. In fact, this architecture can easily be expanded to multiple channels based on a simpler MPPT control algorithm. It has been shown that the total LE count used in the FPGA is low enough that multiple copies could easily fit inside a slightly larger device. Inter-controller communication fabric can remain entirely within the FPGA, decreasing costs and simplifying the design of the whole system.

## VI. CONCLUSION

FPGA-based implementation of an MPPT control system suitable for stereovision robot. At the core of this system, the P&O algorithm is used to track the maximum power point. The algorithm runs on an Altera FLEX 10K FPGA chip. Additional functional blocks, such as the ADC interface, FIR filter, dither generator, and DAC interface, needed to support the MPPT control systems are integrated within the same FPGA device thus streamlining the part composition of the physical prototype of used to build the MPPT control system. Integrating FPGA in an MPPT control system provides numerous advantages. To meet performance requirements, FPGAs are desirable since their performance can easily surpass the performance of microcontrollers and DSPs. Thanks to their high logic capacity, FPGAs can be adapted to control MPPT for multi-channel systems in parallel without imposing complex communication between the individual controls of each channel. In addition, given their reprogrammability, FPGAs can be used to conduct in-circuit experimentation, testing and optimization of various parameters that affect the performance of the MPPT control system. For instance, they can be used to determine an optimal resolution for the ADCs and DACs used in the MPPT control system. By knowing this resolution, only the right components are selected without adding unnecessary costs to the cost of the system prototype. In addition, they can be used to design a suitable filtering scheme to attenuate the effect of noise on the performance of the MPPT control system.

## VII. FUTURE ENHANCEMENT

In addition to their use in stereovision robot, PV arrays are finding a home in terrestrial applications. The thrust to make PV a major component of the world's energy production requires the balance of several major factors. First, the cost of manufacturing the arrays must be low enough to compete with more conventional methods, such as nuclear, coal, and natural gas. Moreover, the implementation and maintenance costs must also be kept to a minimum. In addition, the efficiency must be high in order to harness as much solar energy as possible per unit area. This is particularly important in space-constrained locations, such as residential installations. In every case, the underlying focus is to increase the efficiency of PV technology. Whether the PV array is in an off-grid or grid-connected system, it is usually coupled with an inverter to provide the AC for either residential usage or current injection into the grid. As with any system, ensuring that every component is operating at maximal efficiency is fundamental to achieving high overall efficiency. In the case of PV arrays, their characteristic V-I curve display a maximum-power point which varies with numerous factors including

temperature and insolation. In order to insure that the inverter never attempts to draw more than the maximum power, a condition which would cause the power output to collapse, a MPPT device is used to regulate the PV output. MPPT implementations can vary widely although they all are based on sampling of a combination of current, voltage, and power. A MPPT algorithm is applied to locate and track the global maximum. As the algorithm becomes effective, the control time spent at the top of the characteristic power curve increases. This ultimately determines the efficiency of the MPPT system. However, in real-world implementations, numerous challenges must be overcome in order to perform reliable MPPT. The most daunting problem is the preponderance of noise, which can lead to sampling of false and subsequently incorrect power calculations. In addition, characteristic power curves can contain local maxima beside the desired global maxima. A robust MPPT implementation must be able to overcome these problems in an accurate and robust manner.

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